SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

STV0117A

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1 - SOME DEFINITIONS

To clarify some expressions used in this document :

FRAME : a frame of video is essentially one picture.
In NTSC, a frame of video is made up of 525 individual scan lines.
For PAL and SECAM, it's 625 scan lines.

FIELD : A TV screen is made using two interlaced fields, each one containing half the scan lines needed to make up one frame of video.

CLUT : Color Look up Table
Table containing the digital values for the coding of Cr, Cb and Y components in replacement of R, G, B input data.

DDFS : Direct Digital Frequency Synthesizer
This is a system designed to synthesize tunable high frequency signal.
In fact in the STV0117A, this system generates the chroma subcarrier.

PEDESTAL : this is an offset to separate the active video from the blanking level.
If used, then black level and blanking level are different.
For example, NTSC M uses a 7.5 IRE pedestal (except JAPAN).

VBI : Video Blanking Interval as defined for ST Microelectronics digital encoders.
Frame retrace interval in which lines may be blanked.
2 cases : full or partial

Full Vertical Blanking Interval
NTSC M : lines 1 to 19 and lines 263(half) to 282 (525 SMPTE line number)
PAL M : lines 523 to 22 and lines 260 (half) to 282 (525 CCIR line number)
other PAL: lines 623 (half) to 22 and lines 311 to 335 (625 CCIR line number)

Partial Vertical Blanking Interval
NTSC M : lines 1 to 9 and lines 263(half) to 272 (525 SMPTE line number)
PAL M : lines 523 to 6 and lines 260 (half) to 269 (525 CCIR line number)
other PAL : lines 623 (half) to 5 and lines 311 to 318 (625 CCIR line number)

CtSL : Counter Synchro Loss
In STV0117A, this counter counts up to 3 consecutive frame synchro losts
After this :
- either STV0117A continues in free-run mode (if validated).
- either STV0117A generates only synchro signal (if SyncOK bit validated)
- either STV0117A stops and waits for a new synchronization signal.

2 - GENERAL DESCRIPTION

The STV0117A is a member of the SGS-THOMSON Microelectronics encoder family.

Designed for digital applications, it converts the digital bit stream issued from a video MPEG decoder, into an analog baseband PAL/NTSC signal.

An easy and versatile programmation allows to switch between the various standards like PAL B, D, G, H, I, M, N, and NTSC M.

Output signals are delivered under 2 format types : composite (CVBS) and S-VHS, allowing to cover the maximum of application requirements.

An I/Q specific color processing assures the maximum of image quality in NTSC mode.

27MHz interpolation before modulation assures the maximum of accuracy for the analog video waveform generation, and simplifies the output filtering. Also, a sin x/x correction has been added on luma path.

The test of applications is greatly simplified by an on chip color bar test pattern generator.

Closed-caption interface allows to encode general purpose messages for display at the end user's equipment with a specific decoder.

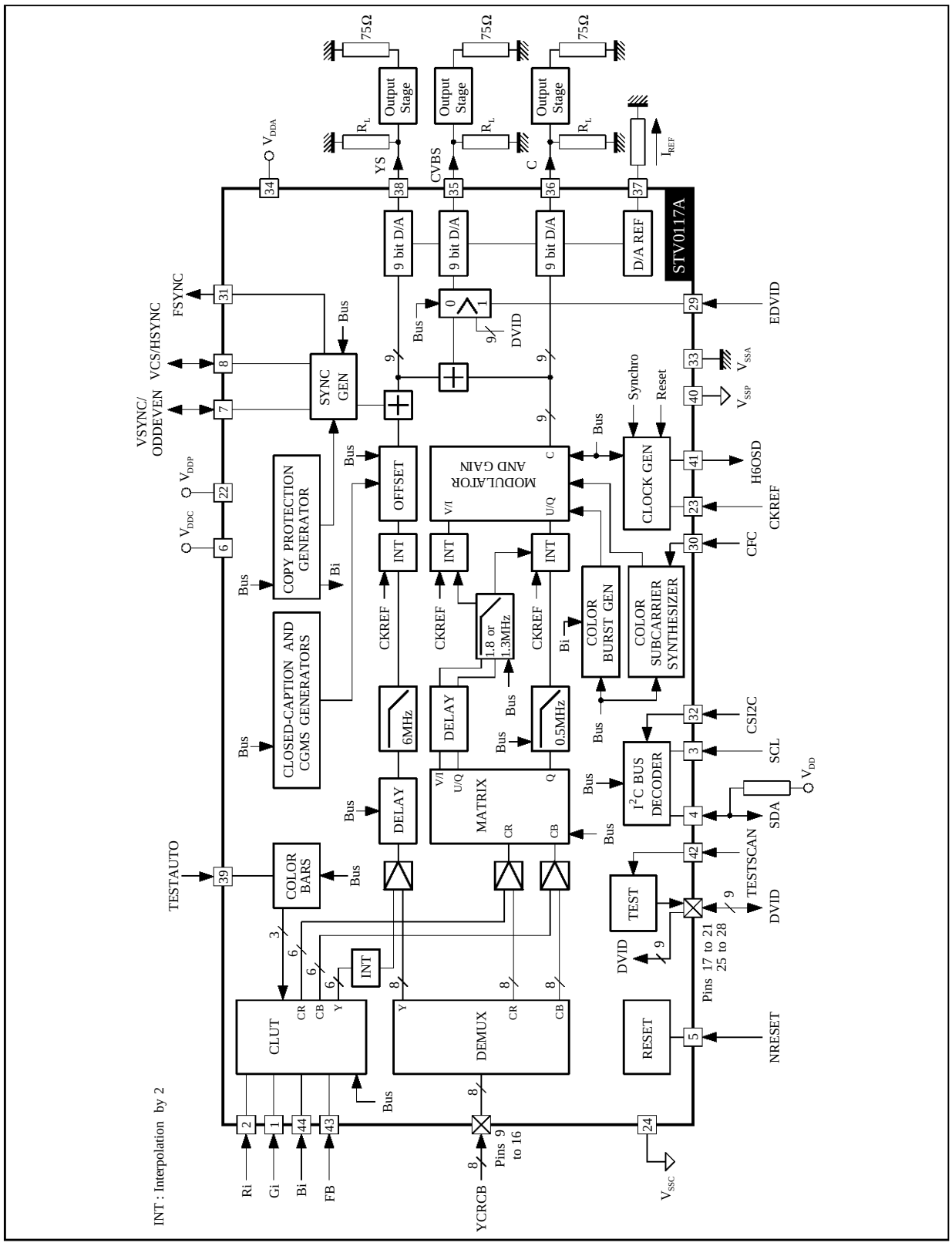
CGMS interface allows to encode data related to various parameters as Copy Protection information, display, format.

An included copy protection generator allows anticopy coding inserted on CVBS, Ys, and C paths. Anticopy coding is MACROVISION™ coding type (versions 6.0 ,6.1 and 7.0 from March 29Th 1996).

Global description of the STV0117A is given in Figure 1.

2 - GENERAL DESCRIPTION (continued)

Figure 1 : Block Diagram



3 - SYNCHRONIZATION

Two main working conditions characterize the STV0117A synchronization monitoring :
- the slave mode, where the STV0117A scans an external synchronization source.
- the master mode, where the STV0117A generates the synchronization signals for the other parts of the application.

3.1- Master Mode

In this mode, the STV0117A generates synchronization signals (ODD/EVEN and HSYNC) for a MPEG circuit, which synchronizes its output multiplexed bus Y/CR/CB on.
This mode is forced by writing in reg 0 (control reg.) bit mod.
In master mode, the STV0117A is always in "Free RUN" mode and the counter "Sync-loss" is always clamped to '0'.

In that case :
- VCS/HSYNC pin outputs a composite synchronization or an horizontal synchronization according to reg 1bit syncsel. VCS/HSYNC pin polarity can be inverted according to reg 0 bit sys1.
- ODD/EVEN outputs a field parity information (if reg 0 sys0 =0) :
  - odd field = low level
  - even field = high level
  ODD/EVEN polarity can be inverted according to reg0 bit sys 0.
- FSYNC outputs a field synchronization for OSD driving purpose (with HSYNC)
  FSYNC polarity can be inverted according to reg 0 bit sys1.

3.2 - Slave Mode

3.2.1 - Slave Mode 1, 2, 3, 4 :

In this mode, synchronization for the STV0117A can be extracted by three ways :
- slave 1 : synchro. extracted from ODD/EVEN input.
- slave 2 : synchro. extracted from EAV (End of Active Video) issued from the multiplexed bit stream (YCRCB).
- slave 3 : synchro. extracted from ODD/EVEN and HSYNC.
- slave 4 : synchro. extracted from VSYNC and HSYNC.

These modes are forced by writing in reg 0 (control reg.) bit mod.
Choice between slave 1/2 or 3/4 being accomplished by reg0 bits sym2 and sym0 and reg4 bit vsyncsel.
- reg0 sym2 = 0 and reg0 sym0 = 0 ==> slave 1.
- reg0 sym2 = 0 and reg0 sym0 = 1 ==> slave 2.
- reg0 sym2 = 1 and reg4 vsynsel = 0 ==> slave 3.
- reg0 sym2 = 1 and reg4 vsynsel = 1 ==> slave 4

3.2.2 - Free Run

In slave mode, is also offered the possibility of "FREE RUN". Thanks to this possibility the user may get an image stable on screen even with a synchro loss.
Reg. 0 bit sym1 allows to enable or disable this mode (bit sym1 = 1 ==> free-run enable).

When operating in "Free Run" mode, two cases have to be considerated :
- slave mode 1 or 2
- slave mode 3 or 4

In slave 3 or 4, as they are line synchronized modes, horizontal synchro loss will clamp all counters and all the logic of the STV0117A. Be aware, in these modes, bits "Free Run" and "syncok" have no meaning.

In slave mode 1 or 2 according to synchro behavior, 3 major processing modes can be distinguished :
- slave mode locked (synchro. is OK)
- slave mode research (synchro loss for less than 3 consecutive frame periods)
- slave mode free run or STV0117A blanked (synchro loss for more than 3 consecutive frame periods)

Figure 2 is describing the slave mode research processing and its consequences on the state of the product.

At the end of the slave mode research, if still there is no synchro detected, then three possibilities are offered according to bits "free run" (reg 0 bit Sym1) and to bit "syncok" (reg 1 bit syncok). Table 1 describes these three states.

Table 1 : STV0117A states in unsynchronized mode

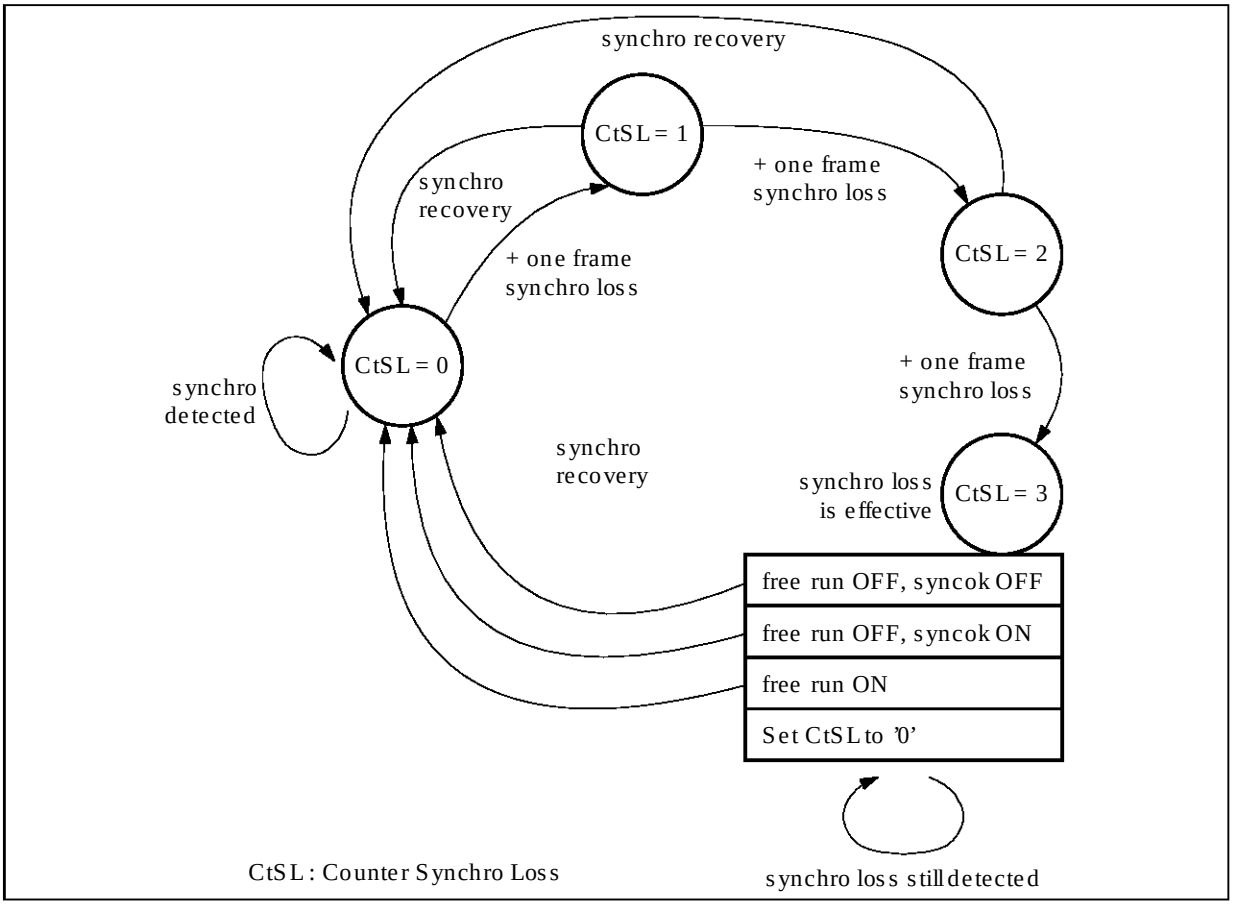
Bit Free Run	Bit Syncok	State Description
0	0	no analog and digital synchro tips, and image blanked
0	1	analog and digital synchro tips, but image blanked
1	0	analog and digital synchro tips, and image not blanked
1	1	analog and digital synchro tips and image not blanked

The return to normal working (slave mode locked) is validated as soon as the synchro signal (ODD/EVEN or F) is back. Then, the sample counter is initialized at "delay reg. value"), and it begins again for normal count according to the standard chosen (from 1 to 1716 for NTSC or 1728 for PAL B/G).

Note : When hard reset is released, the STV0117A is blocked (counters and free run mode inhibited, no synchro tips, no image), waiting for the rising edge of ODD/EVEN and HSYNC input.

3 - SYNCHRONIZATION (continued)

Figure 2 : Slave Mode Research Processing



3.2.3 - Delay Programmation

Again two different operating states have to be considerated according to slave or master mode.

Master mode

The delay programmation goal is to adjust the signal ODD/EVEN with reference to the analog horizontal sync. Delay value is 2's complement coded in reg 5 and 6 allowing positive or negative delay to be fulfilled.

Slave mode

The delay programmation goal is to adjust the data window with reference to incoming data.

In case of slave mode 1 or 2, delay programmation is frame based.
In case of slave mode 3 or 4, delay programmation is line based.

3.2.4 - Synchro-delay programmation

The synchro-delay programmation goal is to adjust the position of the digital synchro output signals (VCS/HSYNC and FSYNC) with reference to the analog video outputs.

This delay is programmable on 12 bits in reg. 7 and 8 (2's complement coded).

Note : Synchro-delay working is disabled in case of slave mode 3 or 4.

4 - OUTPUTS

4.1 - DACs

4.1.1 - DAC General Description

CVBS and SVHS analog outputs are obtained by means of 9-bit D/A converters operating at 27MHz in CCIR601 format (24.5454MHz or 29.5MHz in Square Pixel Graphic format).

All Y, C, CVBS output signals are synchronous with the internal Hsync and Vsync. Thanks to on-chip 3 DACs, they are clocked with the same 27MHz clock (CKREF), and are delivered at the same time.

DAC outputs are current drivers, which may be adjusted by means of the resistor on I_{REF} Pin (Pin 37).
This gives an easy way, to adapt to different output impedances, and to different amplitude requirements. I_{REF} may vary between 2 to 6mA (according to the specification).
When calculated, current drives capabilities show no possibilities to drive 75Ω loads, I.E., a follower able to drive 75Ω will be needed. This could be considerated as a drawback, but in fact it is a design choice, to not implement high current drive capabilities inside the STV0117A, high current drive capabilities being a major risk of image pollution. The fact is, the STV0117A has often been considered as a reference in terms of image quality.

Note : If one of the outputs is not needed (CVBS, Ys, C), to save power consumption, the unused DAC may be switched-off by software :
reg4 bits: downcvbs, downys, downc
= 0 → DAC output normal operation
= 1 → DAC output forced to "0" code

4.1.2 - DAC Load and Reference Calculation

For standard operation mode, it may be suggested to use the DAC at their nominal working current which is about 4mA. I_{REF} = 4mA

As, V_{REF} is about 3V, R_{REF} value will be :

$$R_{REF} = \frac{V_{REF}}{I_{REF}}$$

thus R_{REF} = 750Ω (Normalized value : 750Ω).
But, DAC current gain has to be considered to calculate DAC output load resistor.
DAC current gain is 2.1(according to the specification)

As, $I_{LOAD} = I_{REF} * DAC\ current\ gain$, I_{LOAD} = 8.2 mA

Now, to estimate the DAC output load resistor, it is needed to know the requested output amplitude. Please refer to Figure 3, hereafter.
Voltage needed on DAC output is about 2.7V to be able to drive 1.4V (1.2V for video signal + 0.2V for safety) on 75Ω impedance.

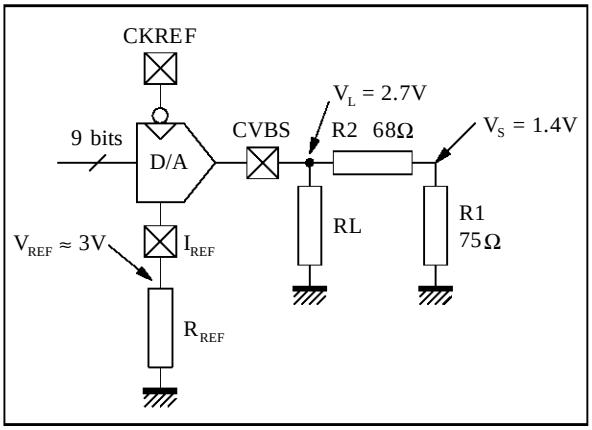
Calculation of Rload is as follows :

$$R_{LOAD} = \frac{V_L}{I_{LOAD}}$$

thus R_{LOAD} = 329Ω (normalized value : 330Ω)

Note : According to the accuracy requested by the application, on video output level, it may be necessary to adapt the accuracy of resistors R_{REF} and R_{LOAD}.

Figure 3 : DAC Output Load Interface



4.2 - Filtering

4.2.1 - Filtering General Description

To simplify the external filtering structure, two kinds of treatments are internally fulfilled :
- a digital high order filtering
- an oversampling, in order to reject the spectrum dubbing in higher frequencies, allowing an external simpler filtering (see Table 2).

An internal "sinx/x" compensation has been implemented on Y filtering path (6.5MHz), to compensate the attenuation of the DAC response at high frequencies.

4 - OUTPUTS (continued)

For the external filtering, only a simple low-pass filter, is needed. For the optimum image quality, the video at output must have a response as flat as possible with a phase shift as little as possible in the useful band. It's why, it is suggested to use an RLC type filter, to have the smallest phase shift (see Figure 4 for the recommended example).

Figure 4 : Recommended RLC Filter

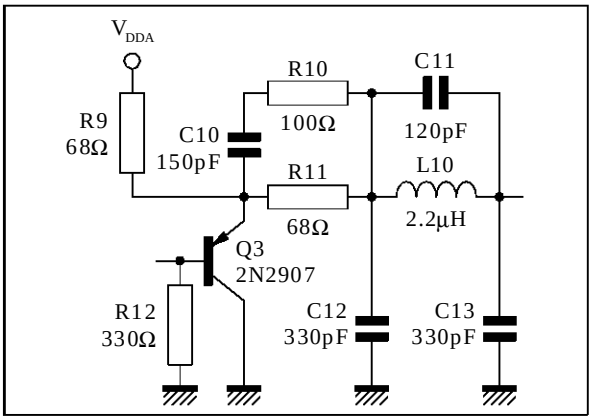


Table 2 : Internal Filtering Description

Output	Filter Type	Structure	Cut Frequency
Y	half band	RIF	6.34MHz
U, V, I	low-pass	RIF	1.3/1.8MHz
Q	low-pass	RIF	0.45/1.8MHz

4.2.2 - Filtering Design

The analog output filter has been designed mainly to offer a better rejection of the spectrum out of the useful band.

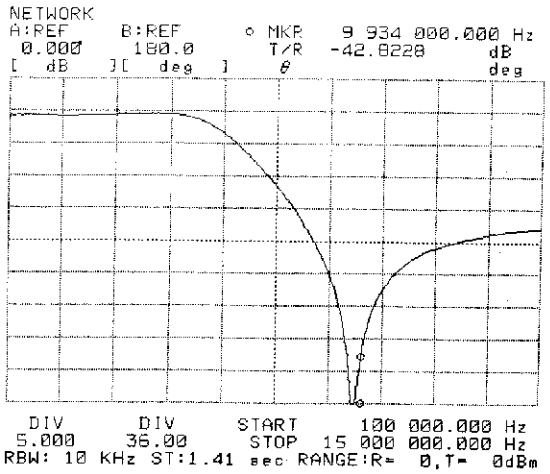
In fact, sampling has for consequence to duplicate the useful spectrum around the sampling frequency (here: 13.5/27MHz), and this duplication may be, according to the encoder following stage, a source of aliasing. That's why it is safe to have a rejection of about 40dB, for all spectrum out of the useful band.

Nevertheless, if for a given application this requirement is not useful, the filtering stage may not be used. By design, the STV0117A is rejecting spurious spectrum at about 25dB.

Design of the filter has been optimized on PSPICE.

Filter response is given on Figure 5.

Figure 5 : Filter Response



The filter response exibits a pole at about 9.5MHz. This pole is created by the capacitor C11 in parallel to the inductor. The aim of this pole is to strongly reject frequencies between 8 and 10MHz, which would not have been possible otherwise.

The RC network R10/C10 acts to emphasize high frequencies in the useful spectrum (to compensate low pass filter (RLC) attenuation) in order to have chroma and luma attenuation as low as possible. This is particularly useful in PAL B/G, I, where the color sub-carrier frequency is 4.43MHz.

5 - STV0117A INTERFACING

5.1 - How to Connect to an OSD Generator?

There are various OSD circuits which may be connected to the STV0117A.

For example :

- STV9420
- STV9424
- STV5730
- ST6xx

The choice between these OSD circuits may be done according to the customer application.

Nevertheless, it may be suggested as standard solution to propose the STV9424, for the main following reasons :

- it is a low cost solution in a 16 pin package
- its character set matrix (12 * 18) is compatible with the Japanese one. The user definable character set will allow to program any specific symbols.
- its software characteristics allow an easy interfacing with the STV0117A
- its reset is a low active reset, as for the STV0117A.
- its I^2C protocol.

OSD connection is made easy, by the fact that a set of digital inputs Ri, Gi, Bi, FB have been implemented on the STV0117A.

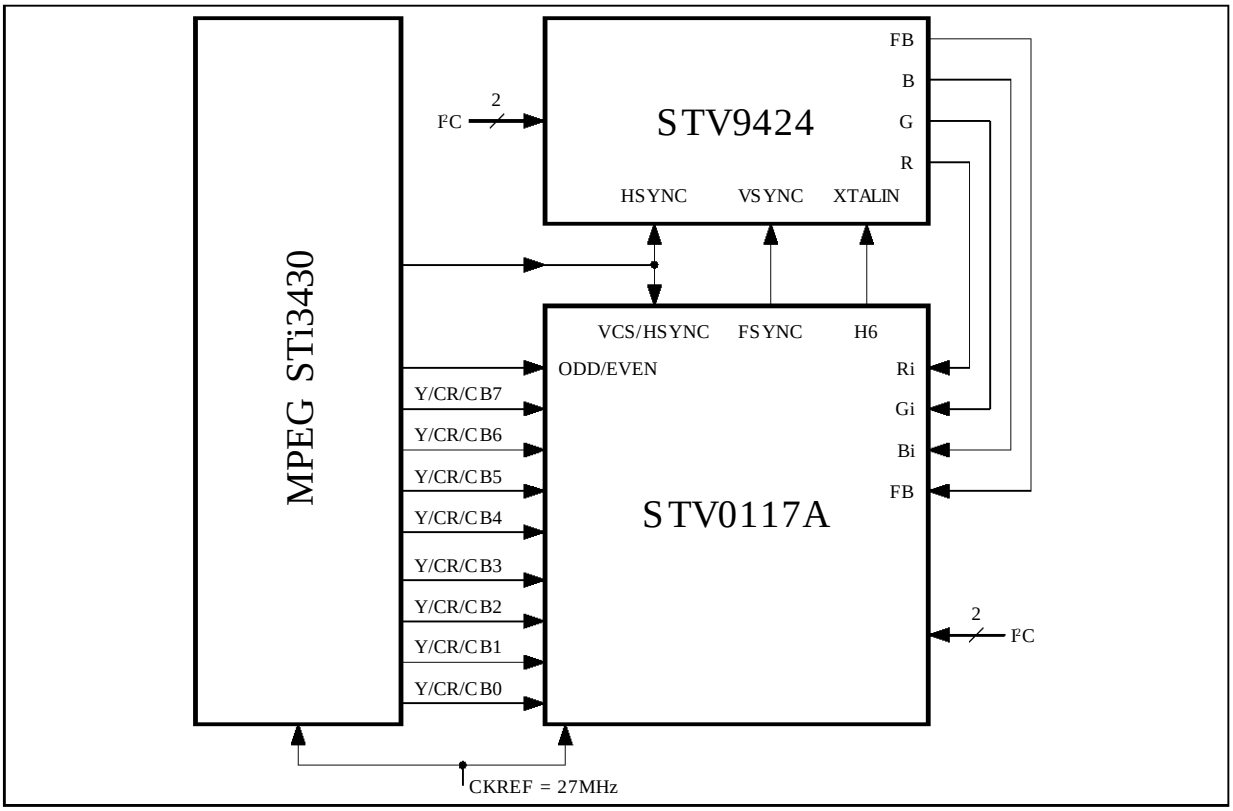
OSD synchronization is achieved by :

- VCS/HSYNC programmed as an horizontal synchro. (reg 1 bit syncsel = 1),
- FSYNC for the vertical synchro.
- and H6OSD enabled (reg 4 bit enh6osd = 1).

On the STV0117A, OSD Ri, Gi, Bi, are transcoded to Y, CR, CB by means of a programmable Color Look Up Table (CLUT). I. E., it is possible to adjust the color of the incrusted OSD by software. More details will be given in the following chapter.

For any specific questions concerning the OSD circuit STV9424, please forward your requests to GRENOBLE VIDEO MARKETING or GRENOBLE VIDEO APPLICATION LAB.

Figure 6 : STV0117A+ OSD Application



5 - STV0117A INTERFACING (continued)

5.2 - How to Adjust the CLUT for RGB Input Encoding ?

OSD CLUT may be programmed by three sets registers :
- reg 15 to 22 : Y clut
- reg 31 to 38 : CB clut
- reg 23 to 30 : CR clut.

On a set of eight registers, each register sets the level of one color (out of sixty four color levels). Each register may be programmed individually or sequentially (refer to Figure 7).

These registers are only 6 bits active registers. As the color coding is defined on 8 bits in the norm CCIR601, an internal expansion to 8 bits is fulfilled. To convert a register value to a normalized value, two "0" must be added on the right of the register value.

ex : register value : 23_h (10 0011xx)
normalized value : $8C_h$ (1000 1100) i.e. 140_d.

5.3 - Autotest Mode

In order to facilitate application design, it has been included inside the STV0117A a color bar pattern generator, designed to conform to CCIR 601 specification. This pattern generator is a 100/0/75/0 color bar type.

Color information is stored in the CLUT, which contains default value on reset.

The construction of Y, CR, CB is based on the following equations giving the normalized values :
- $E'_Y = 0.299\ E'_R + 0.587\ E'_G + 0.114\ E'_B$
- $E'_{CR} = 0.500\ E'_R - 0.419\ E'_G - 0.081\ E'_B$
- $E'_{CB} = -\ 0.169\ E'_R - 0.331\ E'_G + 0.500\ E'_B$

These equations are valuable for analog signals, but for a digital processing, they have to be uniformly quantized on an 8 bit binary encoding.

In respect with the CCIR 601 specification, luminance level will occupy 220 levels, to provide some working margins, and the black level will be 16.

This gives the following equation for y (y sampled) :

$$y = 219\ (\ E'_Y\ ) + 16$$

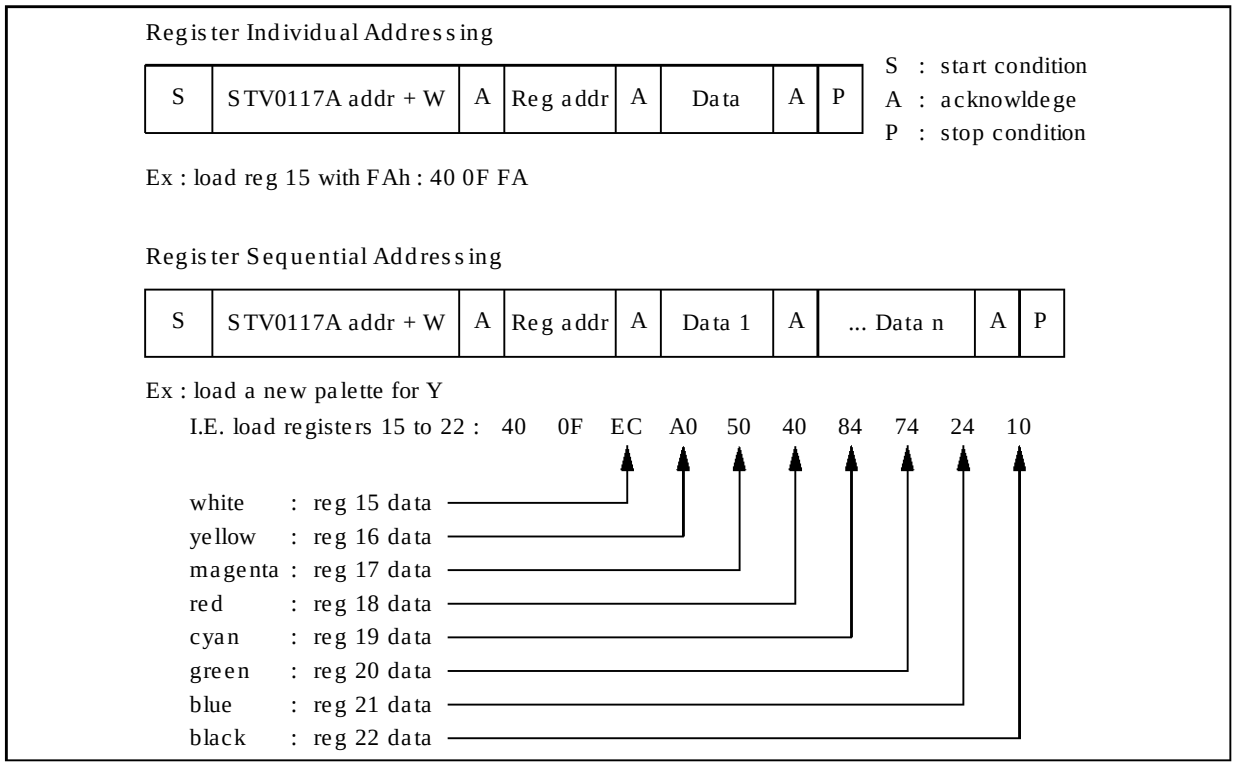
Similarly, the color difference will occupy 225 levels, with the zero level equal to 128.

This gives the following equations for CR and CB :

$$CR = [\ 224.4\ (\ E'_{CR}\ )\ ] + 128$$
$$CB = [\ 224.4\ (\ E'_{CB}\ )\ ] + 128$$

Table 3 summarizes the different values for CCIR 601 normalization.
As on the STV0117A the color coding is defined on 6 bits, Table 4 summarizes the codes implemented.

Figure 7 : I^2C Register Addressing



5 - STV0117A INTERFACING (continued)

Table 3 : CCIR601 : normalization and quantization

Colour	E'_R	E'_G	E'_B	E'_Y	E'_{CR}	E'_{CB}	Y	CR	CB
White	1	1	1	1	0	0	235	128	128
Yellow	0.75	0.75	0	0.67	0.06	-0.38	162	142	44
Cyan	0	0.75	0.75	0.53	-0.38	0.13	131	44	156
Green	0	0.75	0	0.44	-0.31	-0.25	112	57	73
Magenta	0.75	0	0.75	0.31	0.31	0.25	84	199	183
Red	0.75	0	0	0.22	0.38	-0.13	65	212	100
Blue	0	0	0.75	0.09	-0.06	0.38	35	114	212
Black	0	0	0	0	0	0	16	128	128

Table 4 : STV0117Aquantization values

Colour	Y	CR	CB
White	236	128	128
Yellow	160	140	44
Cyan	132	44	156
Green	116	56	72
Magenta	80	196	184
Red	64	212	100
Blue	36	112	212
Black	16	128	128

Autotest pattern generator is available by 2 ways :
- hardware
- software

By hardware : Pin 39 : testauto pin
- = 1 → color test pattern generator ON
- = 0 → normal working mode

By software : Through the I^2C bus, by means of reg 2 bit testauto = 1.
When this bit activates mode testauto, it has priority over the hardware Pin 39.

Enabling the test pattern generator mode will automatically switch the STV0117A to master mode, whatever the previous operating mode.
The user will chose the most convenient solution for his application.

5.4 - MPEG Interfacing

MPEG circuits have to be used with different kinds of synchronizations, which can be easily handled by the STV0117A.

For example :
- with the STi3430, the STV0117A can be synchronized in master or in slave mode as the STi3430 too.
- with the STi3520 or the STi3520A, the STV0117A can only be synchronized in master mode as these MPEG decoders only operate in slave mode.

Figures 8 and 9 shows the STV0117A synchronized in slave mode with an MPEG decoder STi3430.
Two possibilities are offered :
- Synchro. by ODD/EVEN : slave mode 1.
- or synchro. by ODD/EVEN and HSYNC : slave mode 3.

With the STi3430, there is no possibility, to synchronize the STV0117A in slave mode 2, as the STi3430 does not generate ”F” information inside the EAV signal (End of Active Video).

Figure 10 shows the STV0117A synchronized in master mode with MPEG decoders STi3520 or STi3520A.

5 - STV0117A INTERFACING (continued)

Figure 8 : STV0117Ain slave synchro. mode by ODD/EVEN

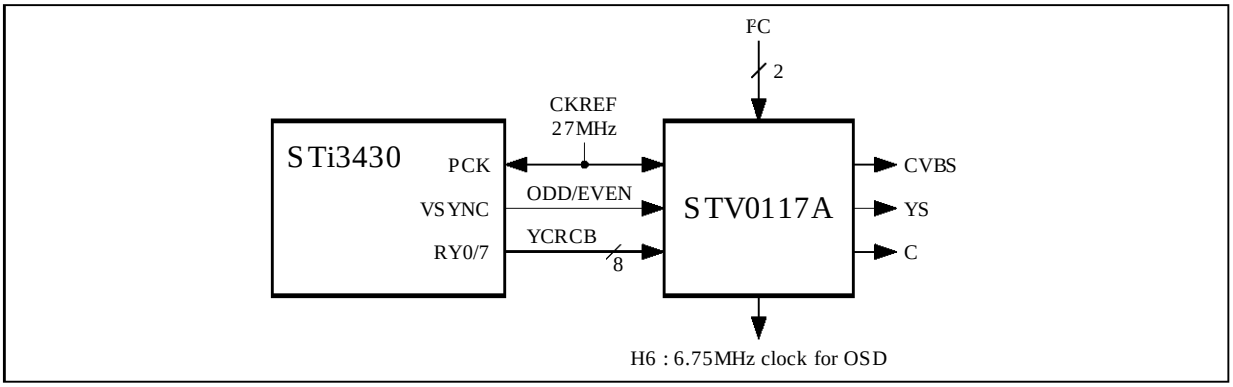


Figure 9 : STV0117Ain slave synchro. mode by ODD/EVEN and HSYNC

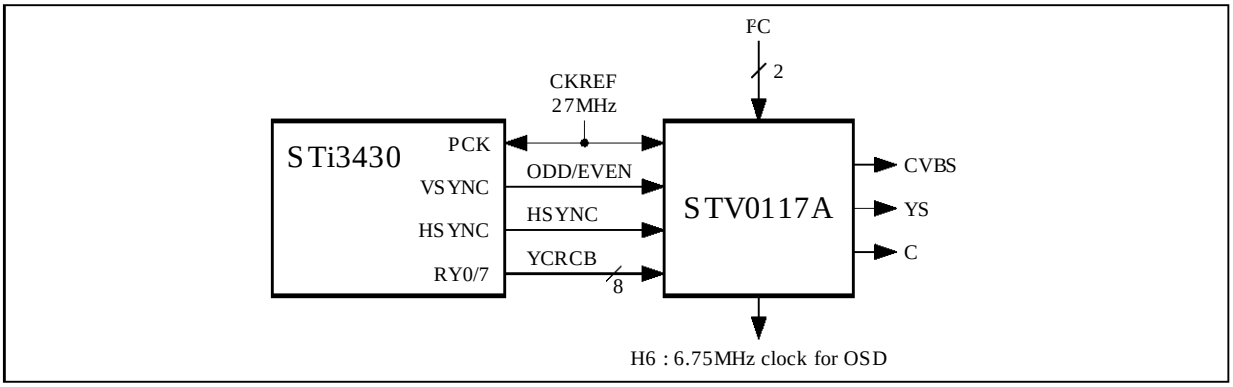
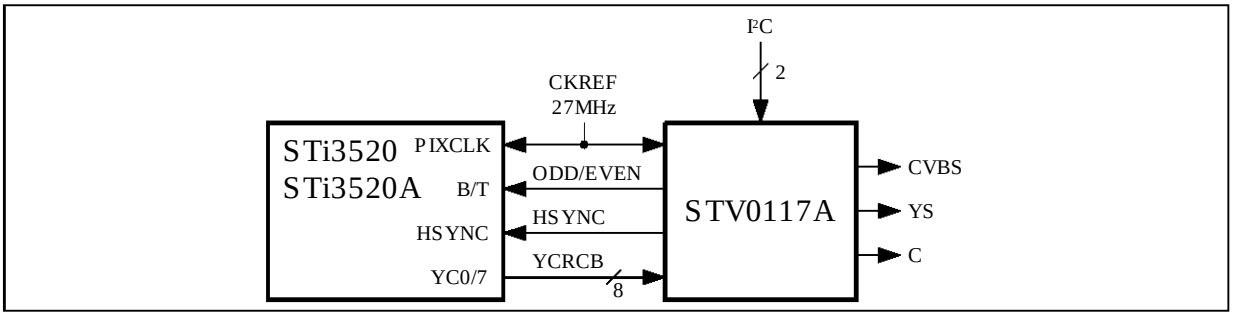


Figure 10 : STV0117Ain master synchro. mode



5 - STV0117A INTERFACING (continued)

5.5 - DVID Interface

This is a 9 bit digital input designed for digitized analog video to access directly to the DAC CVBS input. By means of this interface, the STV0117A can be considered as a digital video switch (refer to Figure 11).

DVID data is latched on the rising edge of CKREF clock. This means that YCRCB or DVID must be SYNCHRONOUS with CKREF.

If two asynchronous video sources have to be used, then the clock must be switched as video input changes (I^2C BUS MUST NOT BE WRITTEN OR READ DURING THE SWITCHING).

Nevertheless, DVID path doesn't include sin x/x correction, this correction being inserted in the luma path before DVID input selection.

Selection between YCRCB and DVID can done by hardware or software.

The choice between both is programmable by I^2C :

- REG3 bit dvids
  0 → software control
  1 → hardware control (EDVID Pin)

The choice of software control will completely inhibit the effect of the hardware control.

If hardware control has been chosen, then the Pin EDVID will allow to select YCRCB or DVID :

- Pin EDVID
  0 → YCRCB
  1 → DVID

If software control has been chosen, then reg 3 bit dvidc will allow to select YCRCB or DVID

- REG 3 bit dvidc
  0 → YCRCB
  1 → DVID

5.6 - I^2C Programmation

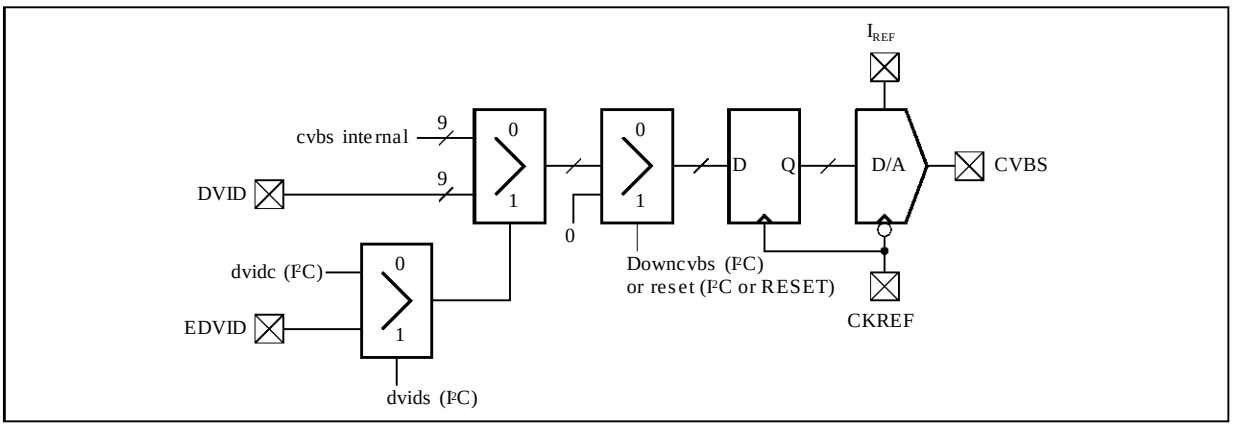
5.6.1 - I^2C Protocol

The STV0117A has an I^2C bus, compatible with both I^2C protocoles. The different ways of addressing the chip are described on Figure 12.

It has to be noted that the STV0117A has even been designed for higher speed I^2C bus than the fast I^2C protocole (max clock freq. = 2MHz).

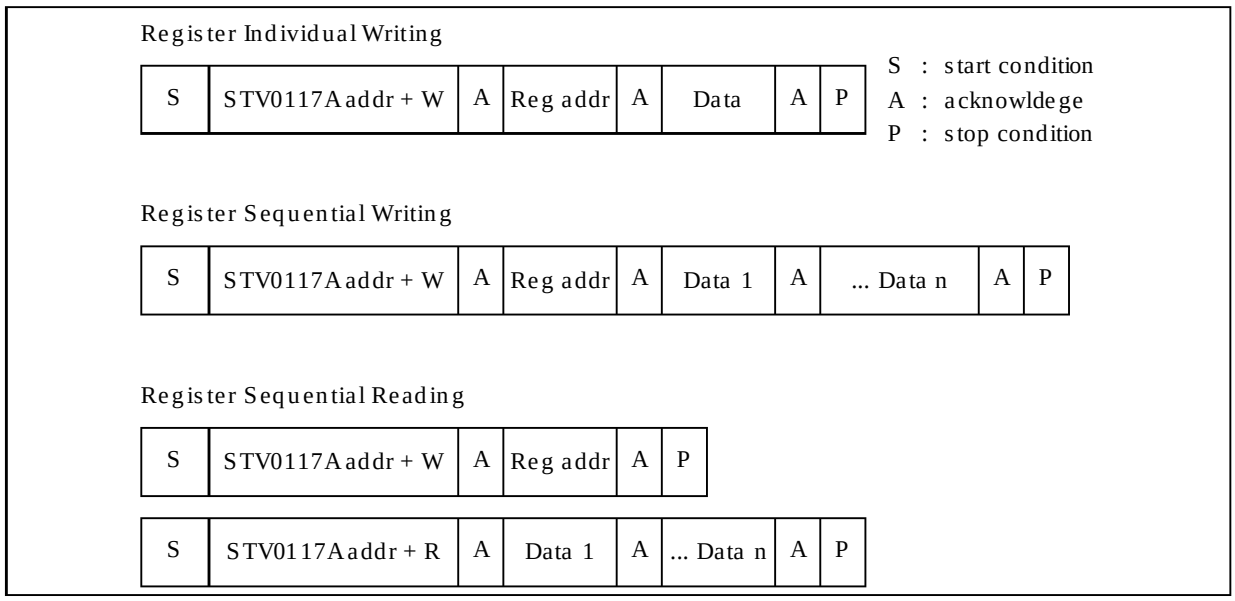
Register configuration has been optimized to improve the programmation efficiency, so to change the standard only a couple of bytes have to be written. Following paragraphs will detail how to take advantage of this feature.

Figure 11 : DVID interface



5 - STV0117A INTERFACING (continued)

Figure 12 : STV0117A I^2C protocol



5.6.2 - I^2C Writing Management with soft reset

Two operating modes can be used :

- mono I^2C register writing.
  Then, the I^2C transmission is like :
  <start/Chip addr./Reg(x) addr./Reg(x) data/stop>
- multiple register writing
  Multiple data may be transmitted in this format :
  <start/Chip addr./Reg(x) addr./Reg(x) data/reg(x+1) data .../stop>

* For mono register writing, the soft reset procedure will be done including the reset active function inside data of reg. 4. There is no need to do a reset active and then to reload register 4 with no reset active included. Even data in this register will be correctly taken into account, because this register is not monitored by software reset, as also registers 9 up to 14.

ex :
<start/Chip addr./Reg(0) addr./Reg(0) data/stop>
<start/Chip addr./Reg(1) addr./Reg(1) data/stop >
<start/Chip addr./Reg(2) addr./Reg(2) data/stop >
<start/Chip addr./Reg(3) addr./Reg(3) data/stop >
<start/Chip addr./Reg(4) addr./Reg(4) (data with softrst=1/stop >
<start/Chip addr./Reg(7) addr./Reg(7) data/stop >
<start/Chip addr./Reg(8) addr./Reg(8) data/stop >

* For multiple register writing, IT IS NOT NEEDED TO STOP the multiple transmission after register 4 as for the STV0117. The loading of the following registers will be correctly accomplished even with a softreset in reg.4.

ex :
<start/Chip addr./Reg(0) addr./Reg(0) data/Reg(1) data/Reg(2) data/Reg(3) data/Reg(4) (data with softrst=1)/Reg(5) data/Reg(6) data/Reg(7) data/Reg(8) data/stop>

5.6.3 - I^2C Routine for a standard change

Thanks to the availability of a versatile software reset procedure, the STV0117A can be controlled in an extremely simple way, giving thus to the users benefits in terms of saving software design resources and ROM code. Therefore, the best way is to take advantage of such software reset, which automatically controls all the sub-processings as :

- the digital frequency synthesizer (frequency and phase offset).
- the delay registers.

Just the following notices have to be taken into account :

- the pedestal is located in register conf1
- the phase reset cycle of the DDFS is located in register conf2.
  It is highly recommended to use the oscillator phase reset every two fields for NTSC (due to COMB filtering in some TV sets).
  But for PAL, it is recommended not to use oscillator phase reset.
- the soft reset is located in register conf4.

As an example, a standard change for the STV0117A is written in Figure13 : It also programs the configuration register 3 for programming simplification, but this is not needed for standard change.

5 - STV0117A INTERFACING (continued)

Figure 13 : I^2C routine for a standard change

```
void Eval3520::InitStv0117(U16  display)
{
U8 control;        // control register value
U8 cfg1;           // config. register values
U8 cfg2;
U8 cfg3;
U8 cfg4;

//-------- this is the STV0117A variable initialization ---------
//
cfg1    = 0xB4;
cfg2    = 0x20;
cfg3    = 0x00;

switch(standard)
  {
  case NTSC:           // for NTSC mode (except: Japan no pedestal)
     control = 0x86;
     cfg2    = 0x21;
  break;
  case PAL_BG         // for PAL B/G
     control = 0x05;
  break;
  case PAL_N1         // For Argentina
     control = 0x05;
     cfg1    = 0xB0;
  break;
  case PAL_N2         // For Uruguay and Paraguay
     control = 0x05;
     cfg1    = 0xB4;
  break;
  default:            // NTSC mode
     control = 0x86;
     cfg2    = 0x21;
  break;
  }
cfg4    = 0x80; // for software reset only (complete validation of the new standard)


//----------- this is the sending on I2C bus -----------
//
// SendI2c is a function which send on I2C bus, chip
// address, register address, data(n).


SendI2c(ADR_WR117A,  CONTROL,&control, 5); //configure 1 control register
                                           //configure 4 config. regiters

//at the end of this routine, for NTSC, following words have been sent on I2C bus
//
// start/40/00/86/B4/21/00/80/stop
}
```

ROUTINE.GEN

6 - VIDEO PROCESSING

6.1 - Chroma Generation

6.1.1 - Color Subcarrier Generator

The color subcarrier generation is fulfilled by a 22-bit digital oscillator which works by adding an increment to an accumulator at a frequency of 27MHz.

Original accumulator value defines an offset which is used to restart counting each time one of the following functions are activated :

- hardware reset which loads the digital oscillator with the values by default (see reg 12/13/14 description for values).
- I^2C writing in reg 2 bit RSTOSC (transition from 0 to 1) which loads the digital oscillator with the values by default or with the values given in the static phase offset registers (reg12/13/14) according to bit SELRST (in reg 2).
- reset every 2/4/8 fields chosen in reg 2 (valrst1 and 2).

Increment reset is activated each time one of the following functions are activated :

- hardware reset which loads the digital oscillator with the values by default (see reg 9/10/11 description for values).
- I^2C writing in reg 4 bit SOFTRST (bit set to 1) which loads the digital oscillator with the values by default or with the values given in the increment registers (reg9/10/11) according to bit SELRST (in reg 2).
- CFC writing with action linked to reg3 bit CFC1 and CFC0 (see following chapter).

The nine MSB of the digital oscillator are used to generate the chroma subcarrier signal, which is defined by its SIN and COS waves.
SIN and COS values are got by reading two ROMs and by adding a sign bit.

For example, for the PAL burst subcarrier generation is using COS values and alternating phase is obtained by changing the sign of the bit each line.

NTSC subcarrier generation is using SIN values with a negative sign.

Notes : - OFFSET Adjustment is only possible over a range of 90°, as the two MSB of the digital oscillator are internally fixed.
- In PAL, there is a limitation in STV0117A cut 1.0: the offset atjustment range is from -37° to -90° and from +54° to +89°. By the way, it is not recommended to use any oscillator phase RESET in PAL. Flickering effects have been observed on some few models of TV sets with short AGC time constants.

6.1.2 - CFC Interface

CFC interface addresses directly the 22 bit digital oscillator, I.E. the increment value (not the offset). This serial interface is operating at CKREF frequency (27MHz).

The protocol is one start bit (0) followed by the 22 bits of the increment (MSB first). Standby level is 1 (see Figure 14).

Information is latched on CKREF rising edge.

Action on digital oscillator is taken into account according to the setting programmed into reg 3 bit CFC1 and CFC0 (see Figure 14).

These 2 bits give 4 different operating conditions :

Bit CFC1	Bit CFC0	
0	0	CFC functionality is disabled
0	1	the increment is updated just after the serial loading via CFC.
1	0	the increment is updated on the next active edge of HSYNC.
1	1	the increment is updated just before the color burst following the serial loading via CFC.

CARE MUST BE TAKEN not to load wrong code as no protection is assumed.

The digital oscillator 22 bit word is calculated as follows :
first LSB value has to be calculated, theoretical value is :

LSB = F(PICLK)/(2**n) F = 27/29.5/24.5454MHz
n = 22 bits

Following results are obtained :

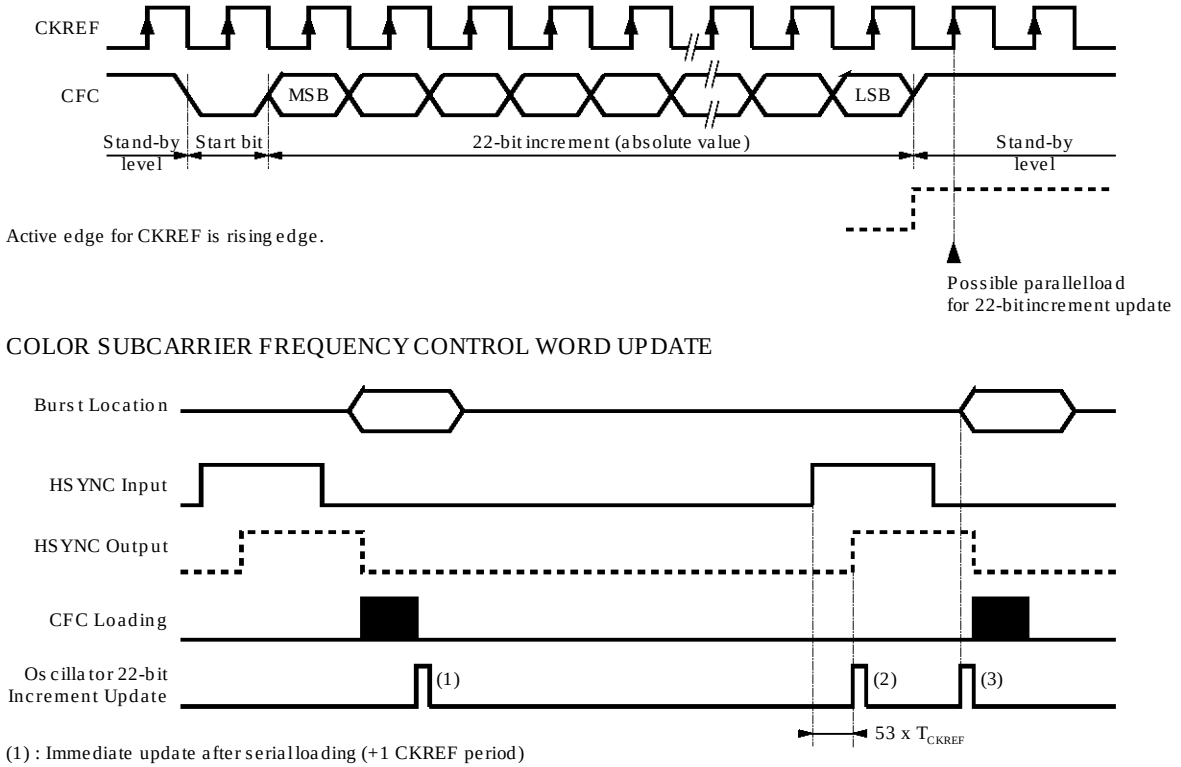
LSB is : 6.4373016Hz for CCIR format
7.0333481Hz for square pixel 625 format
5.8520794Hz for square pixel 525 format

Then, the value to be loaded into the register is :
22 bit word = (Subcarrier frequency/LSB)
Value given in hexadecimal.

For example, the value to be loaded in the register for NTSC is 087C1F (hex).

6 - VIDEO PROCESSING (continued)

Figure 14 : Color Subcarrier Control Word Transmission Format



(1) : Immediate update after serial loading (+1 CKREF period)
(2) : Update on the next line start (HSYNC active edge)
(3) : Update on the next burst start
(0) : CFC word ignored

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6 - VIDEO PROCESSING (continued)

6.2 - Modulation

Here are given some coding laws, for example. This chapter will be detailed in a next revision.

U, V matrixing

U (9 bits) = 0.874*CB + offset
V (9 bits) = 1.230*CR + offset

with the saturation law :
if CR, CB < 16 then CR, CB = 16
if CR, CB > 240 then CR, CB = 240

Q, I matrixing

Q (9 bits) = 0.673*CR + 0.728*CB + offset
I 9 bits) = 1.038*CR - 0.479*CB + offset

with the saturation law :
if CR, CB < 16 then CR, CB = 16
if CR, CB > 240 then CR, CB = 240

Ys law

Y input dynamic range : 16 to 235

In NTSC M (except JAPAN), PAL M,
PAL N (Paraguay, Uruguay) :
Ys = 1.1875*Y +1/+2 + sync
with sync = -40 IRE
blanking level (120) to black level (140) = 7.5 IRE
black level (140) to white level (400) = 92.5 IRE

In PAL BDGHI, PAL N (Argentina) :
Ys = 1.28125*Y -20/-21 + sync
with sync = -43 IRE
blanking level = black level = 128
black level (128) to white level (408) = 100 IRE

6.3 - Interpolation Concept

In the STV0117A, interpolation at 27MHz is fulfilled before modulation. This architecture concept provides a better PAL/NTSC encoding quality and simplifies external filtering structure.
Due to the sampling, which consequence is a duplication of the useful spectrum around the sampling frequency, some spurious frequency spectrum may be present on the subcarrier after modulation, if no care has been taken.
So the useful spectrum has to be extracted by filtering. But, as the sampling frequency is close to the upper frequency of the signal, the separation of the useful spectrum from the duplicated spectrum is not possible without the use of sophisticated filters. Poor filtering consequence is some phase errors and some crosstalk in the modulation.
A way to avoid these problems is to interpolate before modulation

In the STV0117A, the interpolation is performed by some polyphase filters in order to provide :
- interpolation approximating as close as possible the theorical ideal $\frac{\sin x}{x}$ interpolation.
- a high frequency accentuation to compensate the DAC attenuations.

6.4 - Y/C Delay in CVBS mode

STV0117A following stages may add delay between luma and chroma due to filtering phase shifts.
In the STV0117A, this delay is I^2C programmable in the luma path with reference to the chroma path. Reg 3 bits del(3:0) allow to adjust the delay by ±4 steps of 1 pixel clocks cycles (from -296ns, to +296ns by steps of 74ns).

7 - CLOSED CAPTION GENERATOR

7.1 - General Description

The purpose of closed caption is to transmit on the video signal, some information coded in a digital way.

In fact, this information is coded on line 21 of the Video Blanking Interval (VBI) at a rate of 503496.5Hz.

The data signal on line 21 consists of independent data on field 1 and on field 2, each field containing specific data packet types (see Table 5).

Table 5 : Packets transmitted on the different fields

Field 1 Packet	Field 2 Packet
CC1 (Primary Synchronous Caption Service)	CC3 (Secondary Synchronous Caption Service)
CC2 (Special Non-synchronous Use Captions)	CC4 (Special Non-synchronous Use Captions)
T1 (First text service)	T3 (Third text service)
T2 (Second text service)	T4 (Fourth text service)
	EDS (Extended Data Services)

Packet CC1 is the primary language captioning data. It must be synchronous with the sound.

Packet CC3 is the secondary language captioning data.

Packets CC2 and CC4 carries data intended to emphasize information carried in the program, but which does not need to be synchronous with the sound.

Text packets are generally data not program related.

Packets EDS inform the viewer of such information as current program title, length of show,type of show, time in show, or other program related information.

Closed-caption line has the following structure :
- a clock run-in
- three start bits (0, 0, 1).
- two data bytes.

Figure 15 describes a closed-caption line with 2 US-ASCII null characters with odd-parity (as implemented in the STV0117A).

7.2 - STV0117A Implemented Interface

Closed caption interface is composed of three main blocks :
- one for the ”clock run-in” sequence generation.
- one for the shaping and coding of the 2 bytes to be transmitted.
- one for adding both previous signals on the video luma path.

Please refer to Figure 16 for a general description of the closed-caption interface.

Figure 15 : Timing for a closed-caption line

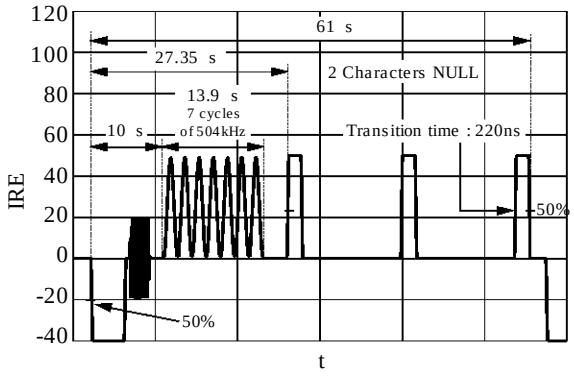
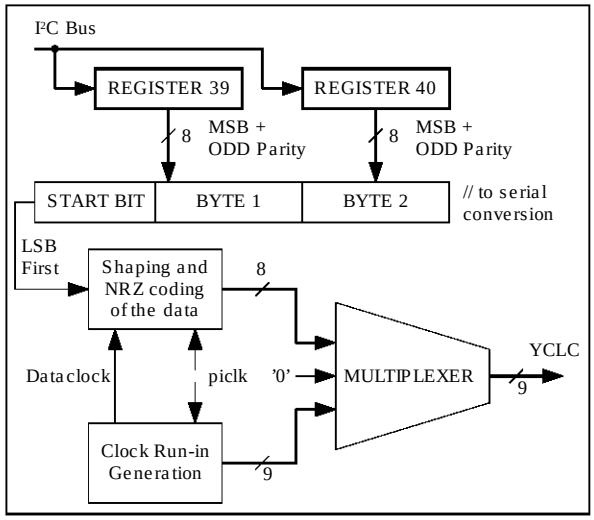


Figure 16 : Closed-caption interface architecture (for field 1)



7 - CLOSED CAPTION GENERATOR (continued)

7.2.1 - "clock run in" Sequence Generation

"Clock run-in" sequence is generated in 7 cycles of a sine wave at 32 times the line frequency.

A clock frequency locked on the clock run-in is also generated by this block for data clocking.

The "clock run-in" generator basically performs Direct Digital Frequency Synthesis. This synthesis is followed by a scaling to comply with the "clock run-in" amplitude requirements. After scaling the "clock run-in" is described on 9 bits.

7.2.2 - Shaping and Coding of the 2 bytes to be transmitted

This block is in charge of generating the controlled-slope NRZ coded data from the 2 US-ASCII bytes stored in the two I^2C closed caption registers.

General operation is as follows: as soon as a pair of data bytes has been written into one of the two pairs of I^2C closed captions registers, data is parallel transferred to a16 bit parallel input serial shift register. When the shift is performed, a 17th bit is added as a start bit.

Shaping required by the closed caption specification, is a 2T pulse shape type.

Design choice was to encode the data bits with a raised-cosine shape.

To be compatible with the luma path, data coding is done on 9 bit basis.

7.2.3 - Adding both previous signals on the video luma path

Both streams ("Clock run-in" and data) are passed through the final multiplexer which, according to time windowing signals (supplied by the synchronization counter) selects either the "clock run-in" stream or the data stream, or blanking levels.

7.2.4 - I^2C programming

Closed-caption data bytes can be loaded anytime (including during line 21) as long as Closed-caption register write rate is once a frame or less. Loading a closed-caption data register twice within less than one frame may be acceptable time to time. At the condition, the rate goes back to once a frame or less immediately after.

BUF1_FREE and **BUF2_FREE** bits in register **STATUS** may also be used.

Notes :
- ODD-parity bit of US-ASCII 7-bit characters is not computed by the interface. I.E. it has to be processed by the microcontroller before it loaded the data bytes in the registers.
- For correct I^2C loading, it is important to always load reg 39 before reg 40 and reg 41 before reg 42.
- No guarantee is given to read I^2C correct values when closed captioning is ON (through reg 39 to 42). I^2C read operations must take place out of closed caption window.
- If Closed-Caption register write rate is less than once a frame, closed-caption data in the output stream will be padded with US_ASCII "NULL" characters.
- Closed-caption registers (reg. 39, 40, 41, 42) reading is one bit right shifted refer to the writing.
  ex : writing : B7 B6 B5 B4 B3 B2 B1 B0
  reading : B0 B7 B6 B5 B4 B3 B2 B1
- By design, closed-caption levels are "set-up" independant.

8 - CGMS GENERATOR

8.1 - General Description

The purpose of CGMS is to transmit on the video signal, some information coded in a digital way.

In fact, this information is coded on lines 20 and 283 of the Video Blanking Interval (VBI) at a rate of Fsc/8 = 447kHz.

The data signal on lines 20/283 is encoded over 20 bits, and carries "Aspect Ratio " or "picture" information in 525 line system. Also, it could be used to transmit information between TV sets and VCRs.

The 20 data bits are divided into three WORDS (0 to 2) and a CRC (see Figure 17).

- WORD0 = 6 bits divided into two parts :
  WORD0-A = 3 bits
  WORD0-B = 3 bits
- WORD1 = 4 bits
- WORD2 = 4 bits
- CRC = 6 bits

Typical CGMS waveform is described in Figure 17.

8.1.1 - WORD0

The purpose is mainly for automatic control at receiver side.

WORD0-A is for transmitted video type information (see Table 6).

WORD0-B is for video related signals, such as audio and so on.

Table 6 : WORD0-A description

Bit N°	"1"	"0"	Comments
1	full mode 16:9	normal mode 4:3	transmission aspect ratio
2	letter box	normal	display type
3	TBD	TBD	

TBD: To Be Defined

8.1.2 - WORD1

WORD1 is for WORD0 related information.

8.1.3 - WORD2

WORD2 is for WORD0 related information.

8.1.4 - CRC

Cycling Redundancy Check coding is a dynamic way of checking the validity of data transmitted on the CGMS words 0 to 2.

This is fulfilled by the polynomial generator :
G(x) = x6+x+1.

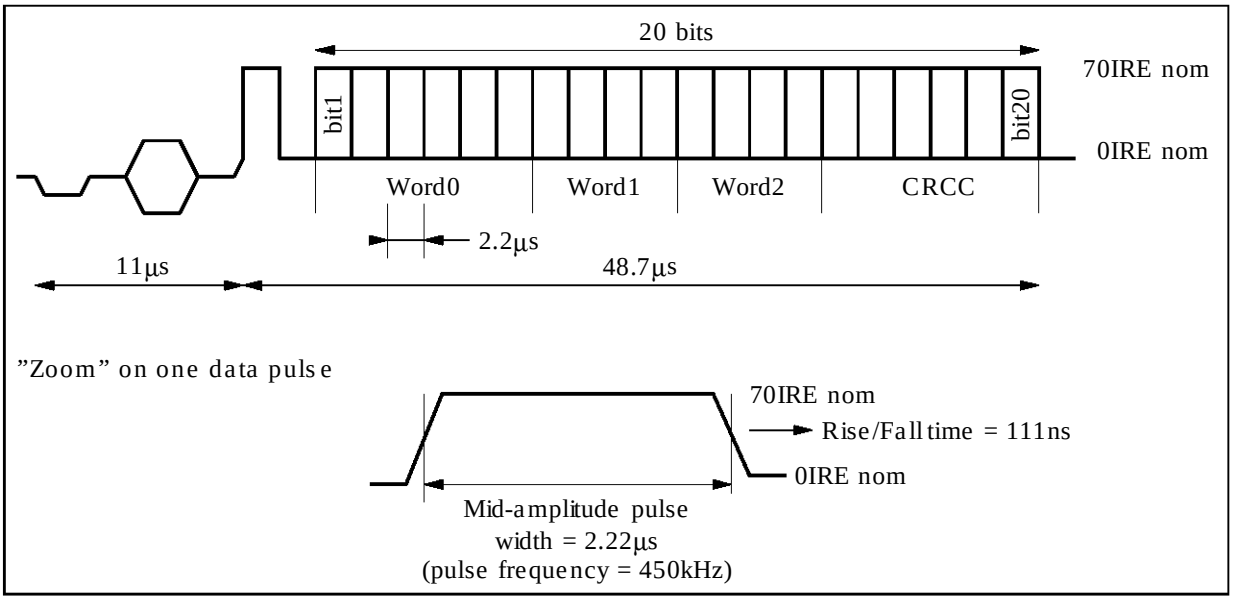
8.2 - Interface Implemented

CGMS interface is composed of 3 main blocks :

- one for the serial bitstream generation
- one for CGMS waveform generation and shaping
- one for adding CGMS signal to the video luma path on the dedicated lines.

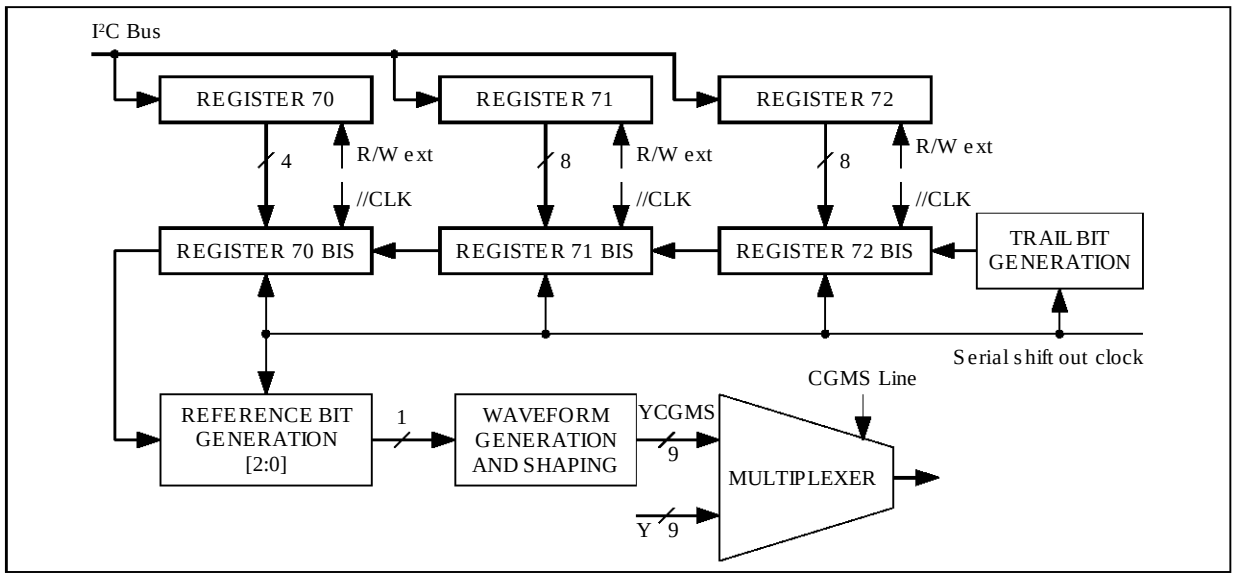
Please refer to Figure 18 for a general description of the CGMS interface.

Figure 17 : Typical CGMS Waveform



8 - CGMS GENERATOR (continued)

Figure 18 : CGMS Interface Architecture



8.2.1 Serial bitstream generation

20 bits out of three I²C bytes (reg70, reg71, reg72) are needed by the interface to encode CGMS data. These bits are firstly in a parallel way, duplicated in three other registers in order to avoid any corrupting risks during the encoding process. Then they are serially processed with other bits to generate the video CGMS bitstream.

To these 20 bits are added :

- 3 front bits: 2 reference bits and one preliminary transient bit.
- 1 trail bit for transient purpose.

8.2.2 CGMS waveform generation and shaping

Level adaptation and shaping are fulfilled by a 2 bits up/down counter.

The 4 bits at the counter output are then padded to 5 preset bits to get the requested digitized video format (9 parallel bits).

8.2.3 - adding CGMS to the video luma path

CGMS bitstream is passed through a final multiplexer thanks to CGMS line windowing signal.

8.2.4 - I²C programming

CGMS data can be loaded any time (including line 20 and 283) thanks to the double-buffered interface.

As CGMS line numbers are programmable via the same I²C registers as those used for closed-caption line programming, CGMS and closed-caption are mutually exclusive in a given field.

Notes :
- CGMS CRCC (Cycling Redundancy Check Code) is not on chip computed, I.E. it has to be calculated by software according to the polynomial generator G(x)= x6+x+1.
- Data registers (reg70, reg71, reg72) have to be loaded in a page like mode, I.E. they have to be loaded as follows : <start/Chip addr./Reg(70) addr./Reg(70) data/Reg(71) data/Reg(72) data/stop>
  No way to load correctly the CGMS data registers, in case of independant register writing.

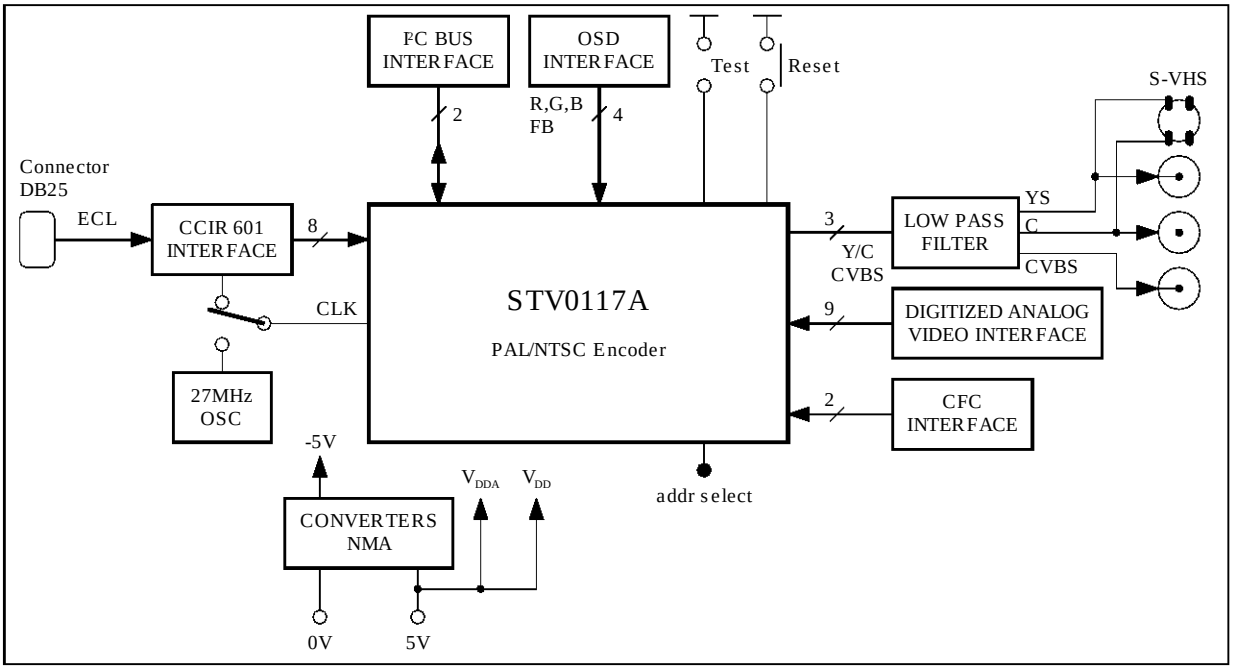
9 - MACROVISION™ COPY PROTECTION SYSTEM

Certainly one of the most interesting part of the product, but as it is under license, nothing about it could be written for a general publication. It will be described in a separate document with restricted access.

Please refer to the specification, to know how to proceed with.

10 - APPLICATION

Figure 19 : STV0117A Application Board Block Diagram



10.1 - Application Diagram

The STV0117A board of SGS-THOMSON Microelectronics has been designed to help the customer to evaluate the performances of the product. Please refer to Figure 19 which describes the block diagram of the board.
A complete schematic of STV0117A application is given in ANNEX 1.

10.2 - Layout Considerations

It is advised to produce a PCB with :

- one Ground plane but taking in account the fact that analog and digital ground MUST have separated layouts, which have to be linked together in a star way.
- one V_{DD} plane but also taking in account the fact that analog digital V_{DD} MUST have separated layouts, which have to be linked together in a star way via isolating inductors (which will also isolate the STV0117A from external high frequency pollutions).

To secure H27 pollution, it may be interesting to include its tracking inside two digital ground tracks.

I_{REF} Pin must be connected as close as possible to ANALOG GND via a resistor. It is also highly recommended to have the shortest connection between R_{REF} and the analog ground pin (Pin 33) of the STV0117A.

Decoupling on Iref may be possible, for a better PSRR (power supply rejection ratio), it is advised to decouple via V_{DDA}.

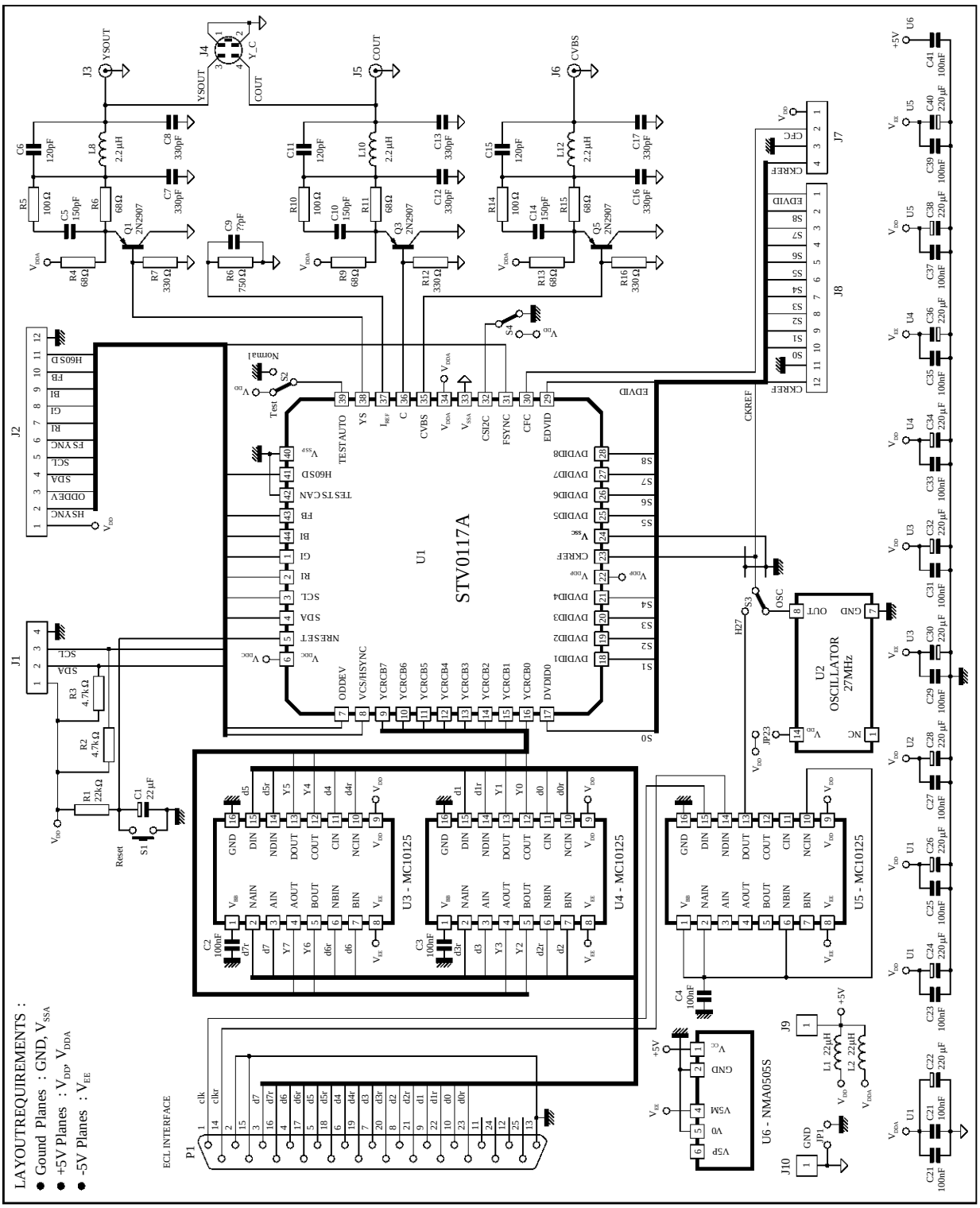
Please refer to ANNEX 2 which details the STV0117A application PCB.

A four layer tracking has been develop for this application

This application kit may be obtained by request to SGS-THOMSON Microelectronics local sales forces . The kit is based on a PC driven software interface controlling the STV0117A application board.

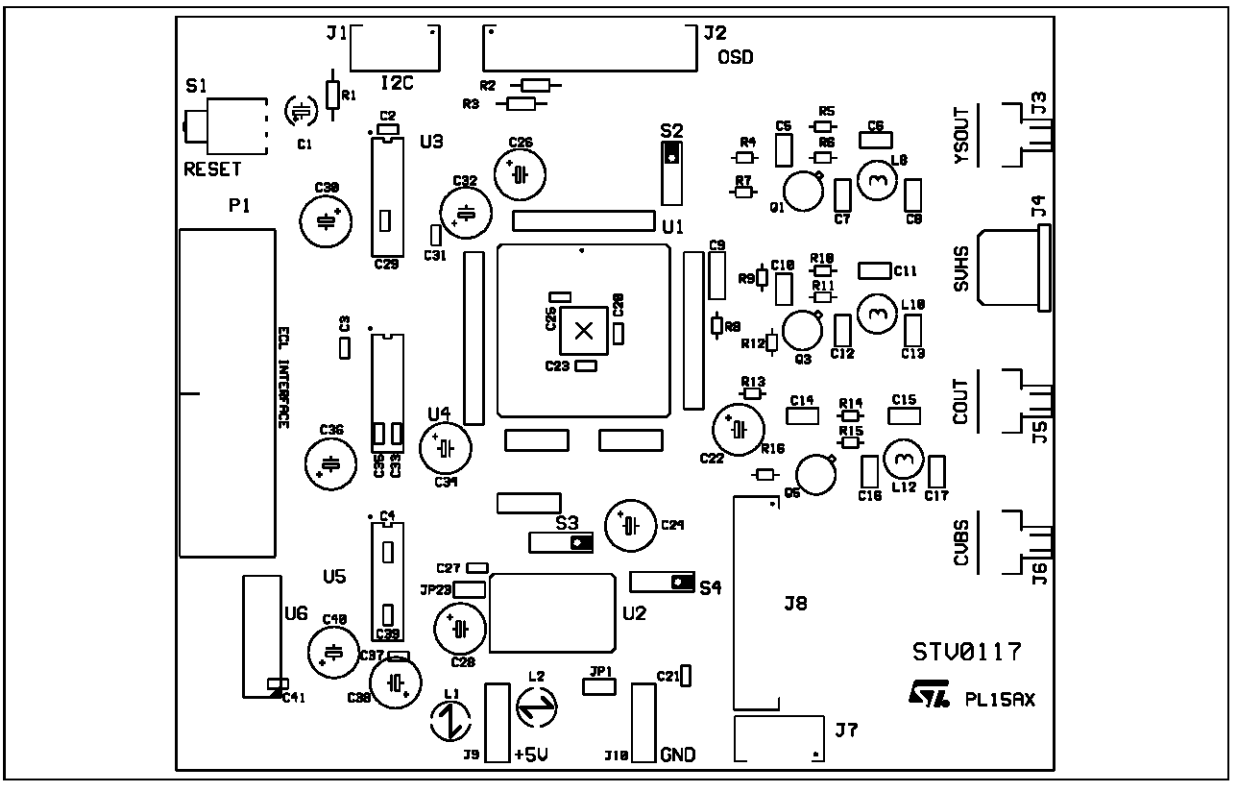
11 - ANNEX 1 : APPLICATION DIAGRAM

Figure 20



12 - ANNEX 2 : APPLICATION PCB

Figure 21 : Serigraphy



12 - ANNEX 2 : APPLICATION PCB (continued)

Figure 22 : Top Layer

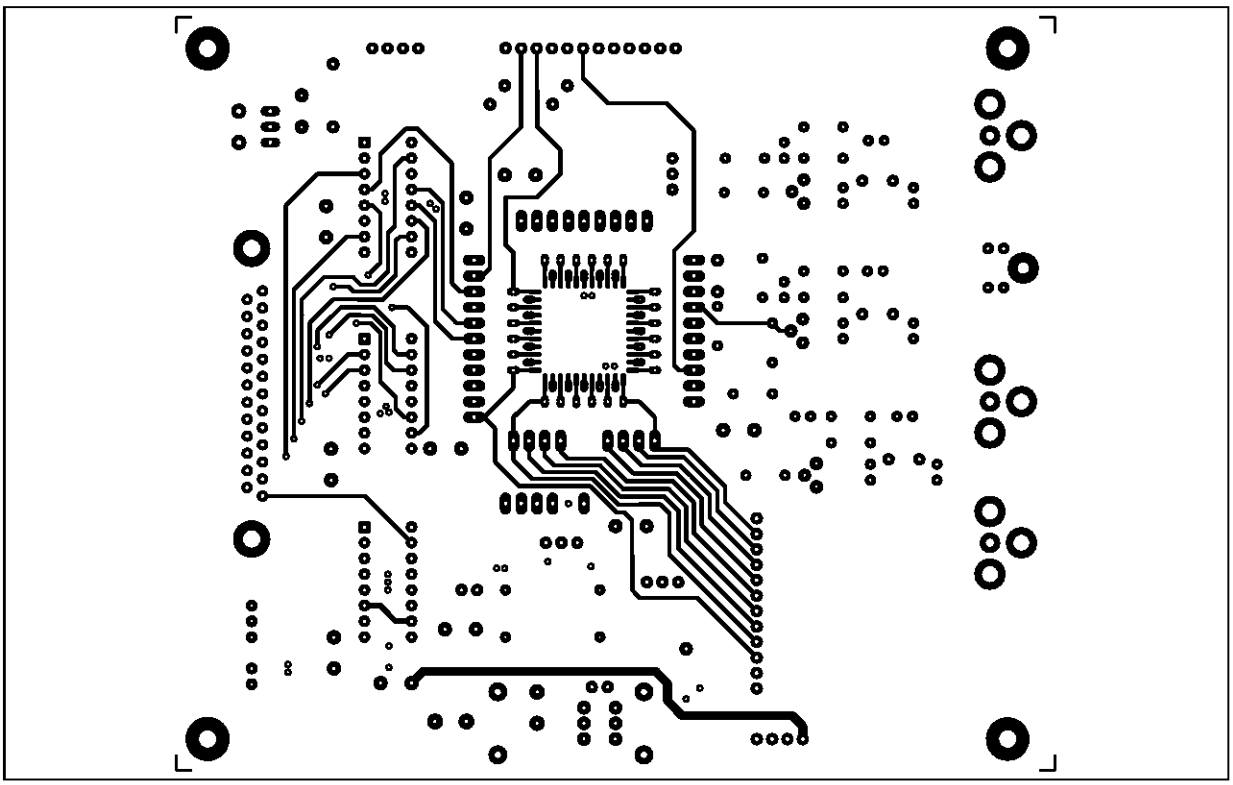
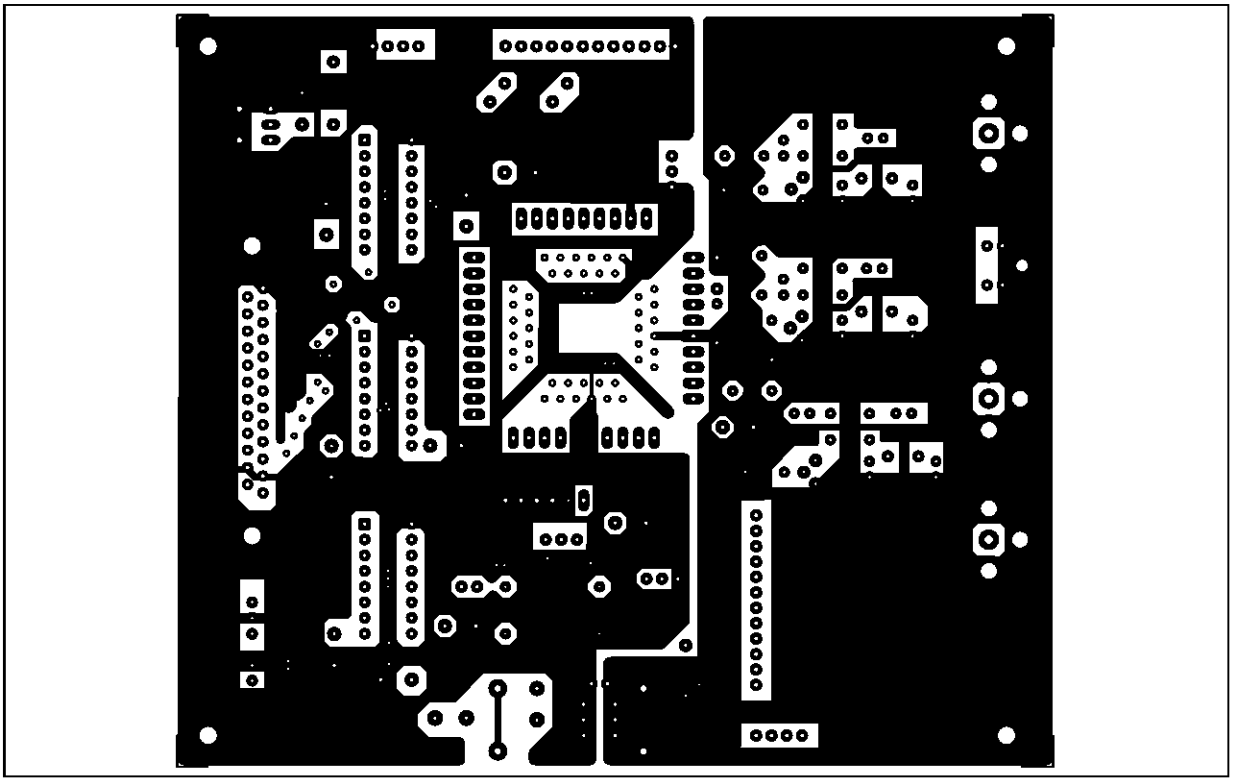


Figure 23 : Ground Plane



12 - ANNEX 2 : APPLICATION PCB (continued)

Figure 24 : V_{CC} Plane

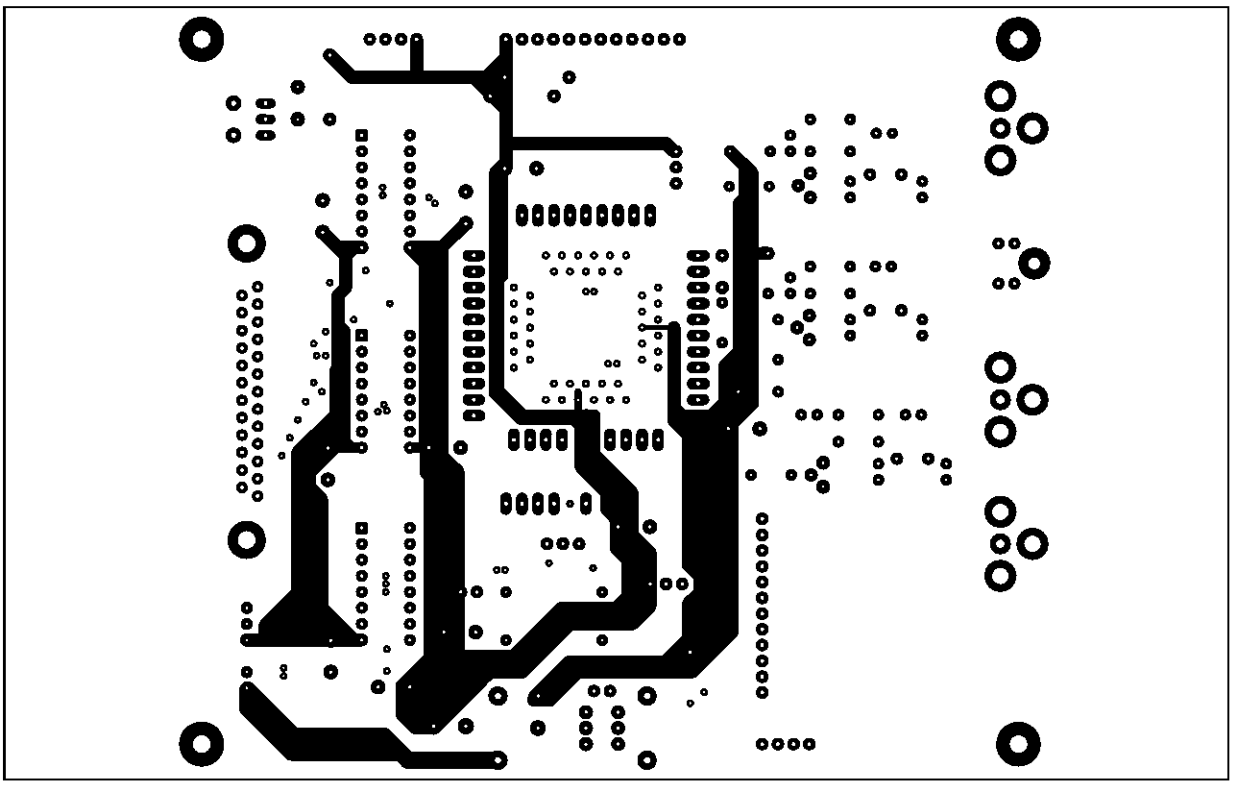


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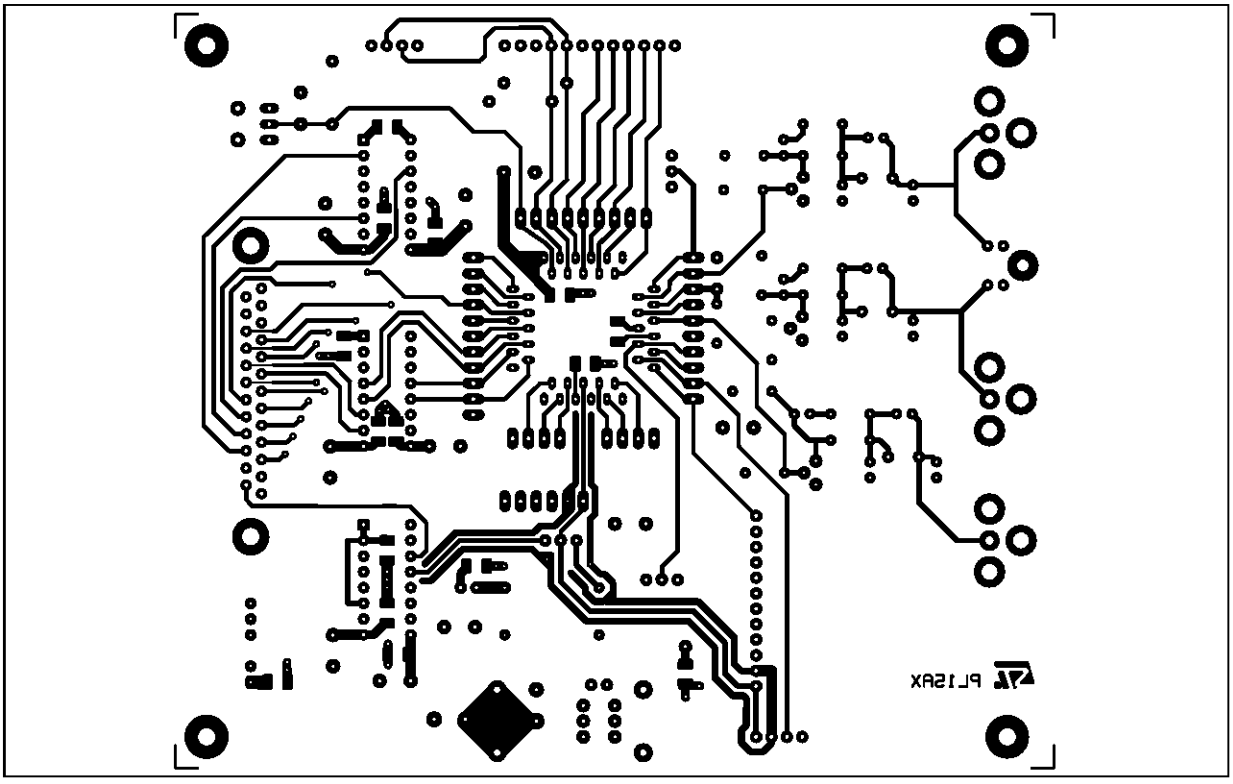
Figure 25 : Bottom Layer



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12 - ANNEX 2 : APPLICATION PCB (continued)

Table 8 : Bill of Materials

Quantity	Package	Value	Components
15	CMSC-8/S0	100nF	C2,C20,C21,C23,C25,C27,C29,C3, C31,C33,C35,C37,C39,C4,C41
10	CHI8	220µF	C22,C24,C26,C28,C30,C32,C34,C36,C38,C40
1	CLC908L	C	C9
1	STO4R	STO4	J1
1	H-LILI	CON1	J10
2	STO12	CON12	J2,J8
1	PHONORCA BIS	YSOUT	J3
1	Y-C VIDEO	Y_C	J4
1	PHONORCA BIS	COUT	J5
1	PHONORCA BIS	CVBS	J6
1	STO4	CON4	J7
1	H-LILI	CON1	J9
2	JUMPER	JUMPER	JP1,JP23
2	VK100	22µH	L1,L2
3	LRADIAL0.2	2U2	L10,L12,L8
1	D-25	DB25	P1
3	TO18BIP	2N2907	Q1,Q3,Q5
1	AXIAL0.4	22kΩ	R1
3	R-1/8	39Ω	R10,R14,R5
6	R-1/4	68Ω	R11,R13,R15,R4,R6,R9
3	R-1/8	470Ω	R12,R16,R7
2	AXIAL0.4	4.7kΩ	R2,R3
1	R-1/8	1.2kΩ	R8
1	POUS H UNI	SW PUSHBUTTON	S1
1	INVUNIP2	INT	S2
2	INVUNIP2	SW SPDT	S3,S4
1	PLCC44	STV0117	U1
1	OSCIL27	OSCILLATOR	U2
3	DIP16	MC10125	U3,U4,U5
1	MINIALI 1W	NMA0505S	U6
1	LOGO0		
1	LOGO1		